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Video/Sound Timing Gate Array: VTG

The VTG implements the horizontal and power supply sync signals, the sound clock, the system timer and the interfaces for the front desk bus modem and the clock chip.

The horizontal and power supply sync signals are derived from the video dot rate clock divided by 32 (ie. 2.1888 MHz) using a six bit counter and write registers 10 thru 13 which provide control of the horizontal period, horizontal blank stop, horizontal sync start and horizontal sync stop. The default at reset provides a horizontal rate of 49.75KHz and a power supply sync at twice the horizontal period at 99.5KHz.

The refresh/sound counter is fixed at four times the sound rate using a divide of 41.5 from the 3.6864 Mhz clock which yields a clock of 88.8 KHz.

The system timer is a 16 bit counter which counts at a rate of one fourth of the 3.6864 Mhz clock (ie. approximately once every microsecond). The timer counts upwards to zero. When the timer rolls over to zero, a time out interrupt is generated (ie. sets SR0) and the system timer is loaded from the the system timer latch (write registers 6 and 7).

The front desk bus (FDB) interface is a five line interface which is controlled by write register 4. The five signals are ST0, ST1, FS7 (data), FC (clock) and FINT. The FDB shift register is located at register 2.

The real time clock (RTC) interface is a four line interface which is controlled by write register 5. The four signals are CINT (1 sec interrupt), RC (clock), CE (clock enable) and RS7 (data).

The VTG is located at $FFFDØØØØ with a register spacing of $10. There are six read registers and ten write registers implemented as follows:

Read Register 0		Status	$FFFD0000
Bit 0	SR0	Status Reg 0, set by the RTC one second interrupt.	
Bit 1	SR1	Status Reg 1, set by the System Timer timeout.	
Bit 2	FINT	FDB Interrupt input.	
Bit 3	RSIN	RTC serial data input.	
Bit 4	RA3	VTG Register Address bit 3.	
Bit 5	ESCE	Enable ENC pin as sound counter enable.	
Bit 6	EOR	Enable output buffer to RTC if set.	
Bit 7	S10	Set if either SR0 or SR1 is set.	

Read Register 2: FDB Shifter $FFFD020
This register allows the FDB shift register to be read.

Read Register 4: Number Low $FFFD040
This register allows the low byte of the number register to be read.

Read Register 5: Number High $FFFD050
This register allows the high byte of the number register to be read.

Read Register 6: Timer Low $FFFD060
This register allows the low byte of the system timer to be read.

Read Register 7: Timer High $FFFD070
This register allows the high byte of the system timer to be read.

Write Register 0: Status $FFFD0000

Bit 0	SR0	RTC one second interrupt bit.
Bit 1	SR1	System Timer timeout bit.
Bit 4	RA3	VTG Register Address bit 3.
Bit 5	ESCE	Enable ENC pin as Sound Counter Enable.

Note: This register must be initialized at system reset.
The remaining bits should be zero when written.

Write Register 2: FDB Shifter $FFFD020 with RA3 reset
This register allows the FDB shift register to be written.

Write Register 4: FDB Control $FFFD040 with RA3 reset

Bit 0	ST0	FDB State 0 control line, set during VTG reset.
Bit 1	ST1	FBD State 1 control line, set during VTG reset.
Bit 2	EOF	Enable output buffer to FDB if set.
Bit 3	OM	Enable inverted clock mode, set for output of data.

Write Register 5: RTC Control $FFFD050 with RA3 reset

Bit 0	CE	RTC enable if low, set during VTG reset.
Bit 1	EOR	Enable output buffer to RTC if set.
Bit 2	RCLK	RTC clock.
Bit 3	RSOUT	RTC serial data output.

Write Register 6: Timer Latch Low $FFFD060 with RA3 reset
This register allows the low byte of the timer latch to be written.

Write Register 7: Timer Latch High $FFFD070 with RA3 reset
This register allows the high byte of the timer latch to be written.

Write Register 10: Period Stop $FFFD020 with RA3 set

This 6 bit register (ie. bits 0 thru 5) can be written to control the period of the horizontal sync and blanking signals. The contents of this register EXORed with 101011 is compared with the horizontal counter to generate the horizontal counter reset.

Write Register 11: Blank Stop $FFFD030 with RA3 set

This 6 bit register (ie. bits 0 thru 5) can be written to control the horizontal blank stop. The start of horizontal blank is always at 0. The contents of this register EXORed with 001011 is compared with the horizontal counter to terminate horizontal blanking.

Write Register 12: HSync Start $FFFD040 with RA3 set

This 6 bit register (ie. bits 0 thru 5) can be written to control the horizontal sync start. The contents of this register EXORed with 101001 is compared with the horizontal counter to enable the start of horizontal sync.

Write Register 13: HSync Stop $FFFD050 with RA3 set

This 6 bit register (ie. bits 0 thru 5) can be written to control the horizontal sync stop. The contents of this register EXORed with 001001 is compared with the horizontal counter to terminate horizontal sync.